

CZ 3001 Advanced Computer Architecture

Name: Kwek Dan Yi, Germaine

Matriculation Number: U1722265L

Lab Group: SS4

**Write the MIPS assembly code for the computation of “d = (a+b)\*(b-c)” with minimum number of instructions.**

LW $1, 1($0)

LW $2, 2($0)

LW $3, 3($0)

ADD $4, $1, $2

SUB $5, $2, $3

MUL $6, $4, $5

SW $6, 4($0)

**Modify the MIPS assembly code for the computation of “d = (a+b)\*(b-c)” for a five stage pipelined architecture given in lab 4, after including NOPs for removing data-dependencies.**

LW $1, 1($0)

LW $2, 2($0)

LW $3, 3($0)

NOP

ADD $4, $1, $2

SUB $5, $2, $3

NOP

NOP

MUL $6, $4, $5

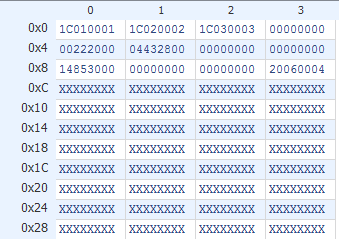
NOP

NOP

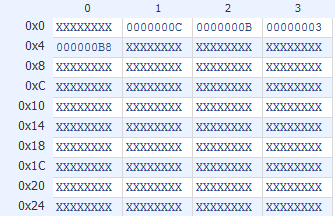
SW $6, 4($0)

**Show the snapshot of instruction and data-memory (all values in hexadecimal) from the ISIM simulation window.**

Instruction Memory:



Data Memory:



**Explain the working of the five stage pipeline both for LW and SW instruction (used in this code) using ISIM window as reference.**

LW Instruction:

Fetch

The Program Counter(PC) holds the address of the next instruction to be executed. The PC passes that address to the Instruction Memory, and the instruction is fetched.

Decode

The opcode is decoded to generate control signals. The source register is passed into the register file, and the data stored in that register(Read Data 1) is read and passed into the ID/EXE pipeline register. The destination register(WriteAddr) is also written into the ID/EXE pipeline register. The offset is then sign-extended to 32 bits and stored in the ID/EXE pipeline register.

Execute

The 32-bit offset will be muxed into the ALU. Read Data 1 is also passed into the ALU. Control signal ALUop will indicate that an addition operation is to be performed. The result is written into the EXE/MEM pipeline register. WriteAddr is forwarded into the EXE/MEM pipeline register.

Memory

MemWrite control signal is set to 0. The ALU result, which is the memory address, is taken from the EXE/MEM pipeline register, and given to the Data Memory. The data is then read from that memory location, but not passed on to the MEM/WB pipeline register. The WriteAddr is passed from the EXE/MEM pipeline register to the MEM/WB pipeline register.

Write Back

Data read from the data memory will be muxed out. This data, along with the WriteAddr from the MEM/WB pipeline register, will be fed into the register file. The data will be written to that specific register identified by the WriteAddr. The loading of data into register is performed successfully.

SW Instruction:

Fetch

The Program Counter holds the address of the next instruction to be executed. That address is given to the Instruction Memory, and the instruction is fetched from that memory location.

Decode

The opcode is decoded to generate the control signals. The source register holding the data to be stored is passed into the register file as Read Addr 2. The destination register holding the base memory address from which the destination memory address will be calculated is also passed into the register file as Read Addr 1. Read Data 1 and Read Data 2 are read from Read Addr 1 and Read Addr 2 respectively and stored into the ID/EXE pipeline register. The offset is sign extended to 32 bits and also passed into the ID/EXE pipeline register.

Execute

Here, we will calculate the destination memory address as it will be used to store the data into the data memory. Read Data 1, which holds the base address, is taken from the ID/EXE pipeline register and given to the ALU. The offset is also taken from the ID/EXE pipeline register and muxed into the ALU. The ALUop control signal will indicate that an ADD operation is to be performed. The result of the addition, which gives the address in the data memory where the data will be stored, will be given to the EXE/MEM pipeline register. Read Data 2, which holds the data to be stored is taken from the ID/EXE pipeline register and given to the EXE/MEM pipeline register.

Memory

The MemWrite signal will be set to 1. The result of the ALU addition will be taken from the EXE/MEM pipeline register and passed into the Data Memory as the Address. Read Data 2 is also taken from the EXE/MEM pipeline register and passed into Data Memory as Write data. Write data will be written to Address. The SW instruction has been successfully performed.

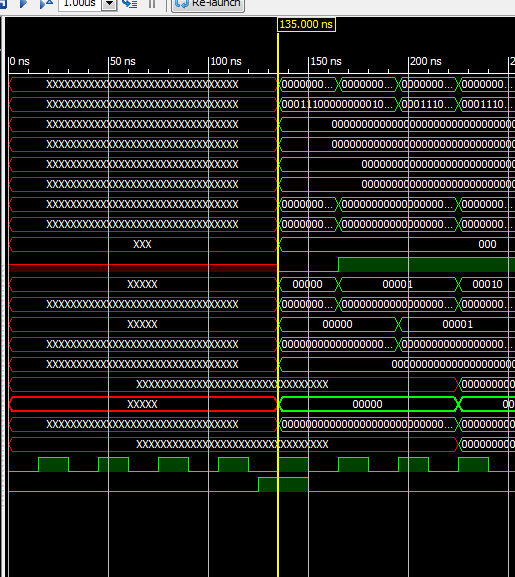
Write-back

No write back required for SW instruction.

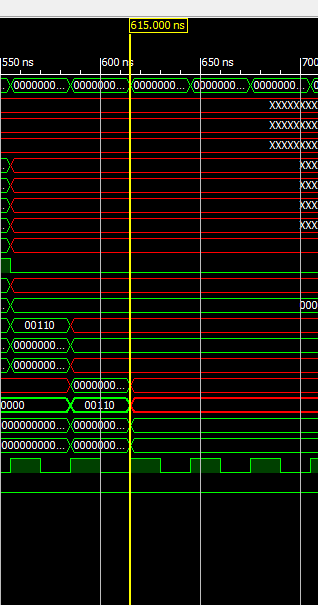
**Indicate the execution time for running this program along with a snapshot of starting and ending time of the code in the ISIM simulator.**

Execution time: 615.000ns - 135.000ns = 480.000ns

Starting time:



Ending time:



**Calculate the steady state CPI of the code while running in a five stage pipelined architecture.**

Steady state CPI

= (number of instructions + number of stalls) / number of instructions

= (7 + 5) / 7

= 12 / 7

= 1.71